What is claimed is:

1. A semiconductor package comprising:

a first conductive layer having a first grid of holes therethrough, the first grid of holes being locatable relative to a first coordinate system;

a second conductive layer parallel to the first conductive layer, the second conductive layer having a second grid of holes therethrough, the second grid of holes being locatable relative to the first coordinate system; and

a plurality of signal traces disposed between the conductive layers, the plurality of signal traces being locatable relative to a second coordinate system, wherein a rotation axis is defined substantially perpendicular to the conductive layers, and the first coordinate system is rotated about the rotation axis between zero and 45 degrees relative to the second coordinate system.

2. The semiconductor package of claim 1, wherein the first coordinate system is rotated substantially 22.5 degrees relative to the second coordinate system.

3. The semiconductor package of claim 1, wherein:

the first coordinate system has an x direction parallel to the conductive layers;

the first coordinate system has a y direction parallel to the conductive layers and perpendicular to the x direction;

the first and second grids of holes include rows and columns of holes, wherein the rows are substantially parallel to the x direction, and the columns are substantially parallel to the y direction; and

the first grid of holes is offset in the x direction relative to the second grid of holes.

4. The semiconductor package of claim 3, wherein the first grid of holes is offset in the y direction relative to the second grid of holes.

5. The semiconductor package of claim 4, wherein the first coordinate system is rotated substantially 22.5 degrees relative to the second coordinate system.

6. The semiconductor package of claim 3 wherein:

the second coordinate system has an x′ direction parallel to the conductive layers, the x′ direction being parallel to the x direction when the first and second coordinate systems are rotated zero degrees relative to each other; and

the plurality of signal traces is substantially routed parallel with, perpendicular to, and at plus or minus 45 degrees to, the x′ direction.

7. The semiconductor package of claim 6, wherein the first coordinate system is rotated substantially 22.5 degrees relative to the second coordinate system.

8. The semiconductor package of claim 6, wherein the first grid of holes is offset in the y direction relative to the second grid of holes.

9. The semiconductor package of claim 8, wherein the first coordinate system is rotated substantially 22.5 degrees relative to the second coordinate system.

10. A circuit device package comprising:

a first conductive layer having a first grid of degassing holes therethrough;

a second conductive layer having a second grid of degassing holes therethrough;

at least one non-conductive layer sandwiched between the conductive layers; and

at least one metal trace proximate to the at least one non-conductive layer, wherein the at least one metal trace traverses a portion of the package at angles of between zero and 45 degrees, 45 degrees and 90 degrees, zero and minus 45 degrees, and minus 45 degrees and minus 90 degrees relative to the first grid of degassing holes.

11. The circuit device package of claim 10 wherein the at least one metal trace traverses at angles of substantially plus or minus 22.5 degrees and plus or minus 67.5 degrees relative to the first grid of degassing holes.

12. The circuit device package of claim 10 wherein the first grid of degassing holes is offset relative to the second grid of degassing holes such that when viewed from a point on a line perpendicular to the conductive layers, the first and second grids of degassing holes form a lattice with degassing holes in the lattice alternating between the first and second grids.

13. The circuit device package of claim 12 wherein the at least one metal trace traverses at angles of substantially plus or minus 22.5 degrees and plus or minus 67.5 degrees relative to the first grid of degassing holes.

14. The circuit device package of claim 10 wherein the first and second grids of degassing holes include rows of holes in a first direction and columns of holes in a second direction substantially perpendicular to the first direction, and wherein the rows are each spaced a first distance from each other, and the columns are each spaced a second distance from each other.

15. The circuit device package of claim 14 wherein the at least one metal trace traverses at angles of substantially plus or minus 22.5 degrees and plus or minus 67.5 degrees relative to the first grid of degassing holes.

16. The circuit device package of claim 15 wherein the first distance and the second distance are substantially equal.

17. Built-up layers for receiving an electronic part, comprising:

a top layer and a bottom layer, the top layer and the bottom layer having a degassing hole configuration comprising a plurality of degassing holes in each of the top layer and the bottom layer, wherein each of the degassing hole configurations are in a grid comprising rows and columns, the rows being in a first direction and the columns being in a second direction substantially perpendicular to the first direction; and

a metal trace sandwiched between the top layer and the bottom layer, the metal trace traversing a portion of the built-up layers at angles of between zero degrees and 45 degrees and at angles of between zero degrees and minus 45 degrees relative to the first direction, and at angles of between zero degrees and 45 degrees and at angles of between zero degrees and minus 45 degrees relative to the second direction.

18. The built-up layers of claim 17 wherein the metal trace traverses at angles of substantially plus or minus 22.5 degrees relative to the first direction, and at angles of substantially plus or minus 22.5 degrees relative to the second direction.

19. An integrated circuit package comprising:

a circuit die; and

built-up layers mounted to the circuit die, the built-up layers comprising:

a top layer and a bottom layer, each of the layers having a plurality of apertures therein, the apertures of the top layer forming a first grid of rows and columns, the apertures of the bottom layer forming a second grid of rows and columns, the rows being in a first direction, and the columns being in a second direction substantially perpendicular to the first direction; and

a metal trace between the first and the second layers, the metal trace running at angles of between zero degrees and 45 degrees relative to the first direction, zero degrees and minus 45 degrees

relative to the first direction, zero degrees and 45 degrees relative to the second direction, and zero degrees and minus 45 degrees relative to the second direction..

20. The integrated circuit package of claim 19 wherein the metal trace runs at angles of substantially plus or minus 22.5 degrees relative to the first direction, and at angles of substantially plus or minus 22.5 degrees relative to the second direction.

21. A circuit assembly, comprising:

a microprocessor;

a substrate, comprising:

a first layer and a second layer stacked substantially on top of one another, each of the first and second layers having a plurality of apertures therein, the aperture positions in the first layer and in the second layer forming rows and columns, the rows being in a first direction, and the columns being in a second direction substantially perpendicular to the first direction; and

a metal trace between the first and the second layers, the trace running at angles of between zero degrees and 45 degrees relative to the first direction, zero degrees and minus 45 degrees relative to the first direction, zero degrees and 45 degrees relative to the second direction, and zero degrees and minus 45 degrees relative to the second direction; and

a motherboard having a plurality of mounting areas thereon, the substrate and the microprocessor being mountable on the motherboard.

22. The circuit assembly of claim 21 wherein the metal trace runs at angles of substantially plus or minus 22.5 degrees relative to the first direction, and at angles of substantially plus or minus 22.5 degrees relative to the second direction.

23. A microprocessor comprising:

a microprocessor semiconductor die having input/output nodes; and

a package configured to receive the microprocessor semiconductor die, wherein the package includes built-up layers comprising:

a first conductive layer having a first grid of degassing holes therethrough;

a second conductive layer having a second grid of degassing holes therethrough;

at least one non-conductive layer sandwiched between the conductive layers; and

at least one metal trace proximate to the at least one non-conductive layer, wherein the at least one metal trace traverses a portion of the package at angles of between zero degrees and 45 degrees, 45 degrees and 90 degrees, zero degrees and minus 45 degrees, and minus 45 degrees and minus 90 degrees relative to the first grid of degassing holes.

24. The microprocessor of claim 23 wherein the at least one metal trace traverses at angles of substantially plus or minus 22.5 degrees and plus or minus 67.5 degrees relative to the first grid of degassing holes.

25. The microprocessor of claim 23 wherein the first grid of degassing holes is offset relative to the second grid of degassing holes such that when viewed from a point on a line perpendicular to the conductive layers, the first and second grids of degassing holes form a lattice with degassing holes in the lattice alternating between the first and second grids.

26. The microprocessor of claim 25 wherein the at least one metal trace traverses at angles of substantially plus or minus 22.5 degrees and plus or minus 67.5 degrees relative to the first grid of degassing holes.

27. The microprocessor of claim 23 wherein the first and second grids of degassing holes include rows of holes in a first direction and columns of holes in a second direction substantially perpendicular to the first direction, and wherein the rows are each spaced a first distance from each other, and the columns are each spaced a second distance from each other.

28. The microprocessor of claim 27 wherein the at least one metal trace traverses at angles of substantially plus or minus 22.5 degrees and plus or minus 67.5 degrees relative to the first grid of degassing holes.

29. The microprocessor of claim 28 wherein the first distance and the second distance are substantially equal.

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